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SKA Management Board description Board revision 1.1

Written by
Sandro Pastore

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1. SCOPE

Purpose of this document is to introduce the designer to the Management Board of SKA (Square Kilometer Array), providing information about the board components, the main functions and interfaces, the mechanical, electrical, power characteristics and the board start-up.

The document is organized as follows: an overview, the board mechanical and electrical characteristics, the main features, interfaces and interconnections among main building blocks (the complete pinout and connection table of the larger devices are available), information about power consumption, configuration details of the main programmable devices, description of the board power up sequence.

This document refers to revision 1.1 of the board schematics.

2. ACRONYMS

AD	Analog to Digital	Mbps	Mega bits per second
ADC	Analog to Digital Converter	MIPS	Million of Instruction Per Second
CPLD	Complex Programmable Logic Device	PLL	Phase Locked Loop
CPU	Central Processing Unit	PPS	Pulse per second
COTS	Commercial Off The Shelf	QSFP	Quad Small Form-factor Pluggable
DDR	Double Data Rate	RAM	Random Access Memory
EEPROM	Electrically Erasable PROM	SDRAM	Synchronous DRAM
FPGA	Field Programmable Gate Array	SPI	Serial Peripheral Interface
HDL	Hardware Description Language	SRAM	Static RAM
HW	Hardware	STD	Standard
IF or I/F	Interface	SW	Software
IO or I/O	Input/Output	SKA	Square Kilometer Array
IP	Intellectual Property	TBC	To Be Confirmed
ITPM	Italian Tile Processor Module	TBD	To Be Defined
MAC	Media Access Control	UDP	User Datagram Protocol

3. APPLICABLE AND REFERENCE DOCUMENTS

3.1 APPLICABLE DOCUMENTS

[AD1] SKA-TEL-LFAA-0500001 SP-COR-DD Rev 01 Signal processing design document.pdf
[AD2] inaf_capitolato_smm_310517.pdf
[AD3] SKA-TEL-LFAA-0500035_LFAA_SPS_DDD Report_20181025 re-sign – signed.pdf
[AD4] 2018_03_29_PCB_Management_1_0.dxf

3.2 REFERENCE DOCUMENTS

[RD1] SKA_Subrack_mechanical.pdf – mechanical PCB drawing (to be delivered)
[RD2] SKA_MANAGEMENT_rev0.1.pdf - board preliminary schematic
[RD3] SKA_MANAGEMENT_V01_Components_Main.xls – board preliminary component list
[RD4] SKA_MANAGEMENT_PowerEffort.xls – preliminary power budget
[RD5] DDD_Cabinet_performances.pdf
[RD6] Cabinet monitor and control point.pdf

4. OVERVIEW

The SKA Management Board integrates the TPM service functions required at Rack and Subrack level with Hi-Level command interface with the telescope manager application.
The Management board is proposed with two possible configurations, Rack and Subrack with combined functions.
In the Rack configuration the Management board is boxed in a 1U drawer to provide the following main functions:

- Interface with the SKA 40G Ethernet network
- Provide the Rack level 1G local Ethernet network
- Interface with the SKA 10Mhz & PPS Rack synchronization signals and distribute them in the Rack
- Provide a Linux-based CPU to execute high level Rack function
- Monitor and manage the cabinet level cooling system
- Interface all rack element for remote control operation and monitoring

In the Subrack configuration the Management board is plugged on the backplane to provide the following main functions:

- Interface the Rack Ethernet network to all the TPM
- Distribute or regenerate the synchronization signal to all the TPM
- Manage and monitor the Subrack power supply and the power distribution to all the TPM
- Manage and power the FANs for the Subrack air cooling system
- Provide a Linux-based CPU to execute high level Subrack function
- Provide the Ethernet network interface for the Remote Field Station

For the above mentioned functions the backplane board extends the functions for the mechanical interface, power distribution and clock distribution functions.

The following list sums up the remarkable Management characteristics and features:

- 6U size format compatible, 350 mm depth
- Single supply, 12 DC input
- 1x4 High Quality passive 10Mhz clock distribution (differential)
- 1x4 PPS distribution (single ended)
- Digital PLL High Quality 10Mhz re-generation and PPS encoding/decoding
- One 40G Ethernet interfaces (QSFP) with only one 10G Ethernet active
- Up to 18 port Ethernet Gigabit Switch with 10G Uplink
- Two Ethernet gigabit SFP interfaces, alternate to the 10G Uplink function
- Low-level Ethernet gigabit management interface with instant ON flash based Lattice CPLD

- Hi-performance CPU ARM9 based, dual core running @ 1Ghz with enhanced capabilities
- Solid state 4GByte FLASH system memory, for OS and data
- Four DDR3L, 64 bit memory banks, 1 GByte total size running @ 1Ghz
- SD card slot for FLASH memory expansion
- Two USB 2.0 and HDMI output for additional User Interface
- CPU trace port available on a high speed connector for SW debugging
- Complete system monitor CPU with power, voltage and temperature monitoring
- 256Mbit SPI user FLASH
- Two I2C board temperature sensors
- Two EEprom for board configuration data with pre-assigned MAC address
- Expansion GPIO connector with UART, CAN, SPI, I2C, PWM available functions
- SATA II interface connector for hard disk storage capabilities
- PCI Express 1x interface for expansion capabilities
- Interface for external battery pack

MECHANICAL OVERVIEW AND BOARD LAYOUT

4.1 Mechanical Overview

The Management fits a 6U high and 379 mm depth rack mount format, compatible with next iTPM 1.5 defined layout [AD4].
The Rack configuration connectors are grouped on the front side, the Subrack ones are on the two lateral sides.
A preliminary overview of the board mechanical layout top view is available in Figure 1

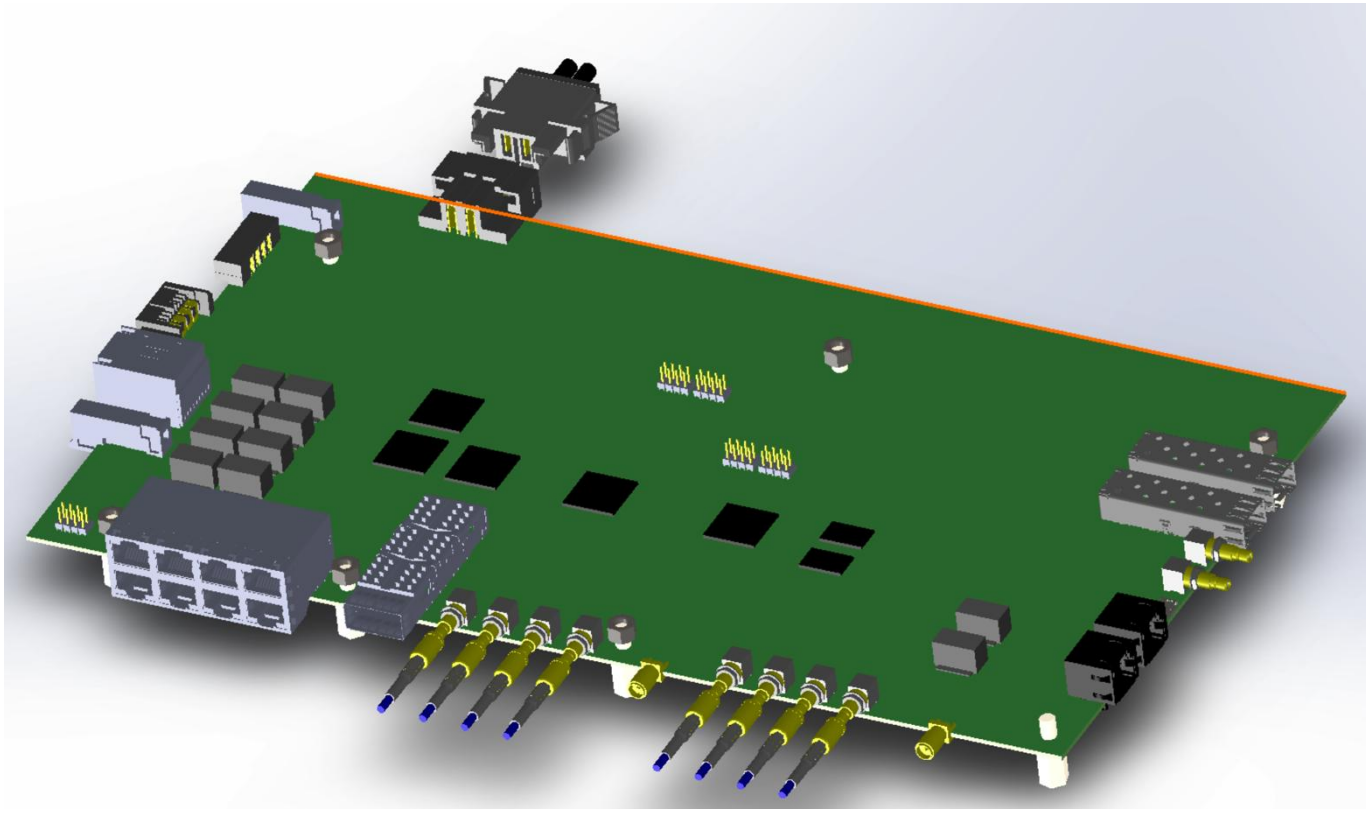


Figure 1. Management TOP preliminary mechanical layout

In the “Backplane” side of the board, on the left in the image, scalable configuration is provided for a x8 TPM or x12TPM Subrack configuration. The three connector in the center of the side are required for both configuration, the two connectors on the margin are not required only for the x12 TPM configuration.

The board will be designed to avoid active dissipation in a controlled temperature environment. In the 1U drawer and in the Backplane a low speed air circulation shall be sufficient for heat sink dissipation.

In the bottom side only low profile components are present without significant power consumption.

4.2 Board Layout

Board Layout is organized with function specialized areas for optimal layout and performances. The clock areas are considered RF circuit and separated from the possibly noise sources high speed digital circuits, with the same approach successfully adopted on the iTPM board.

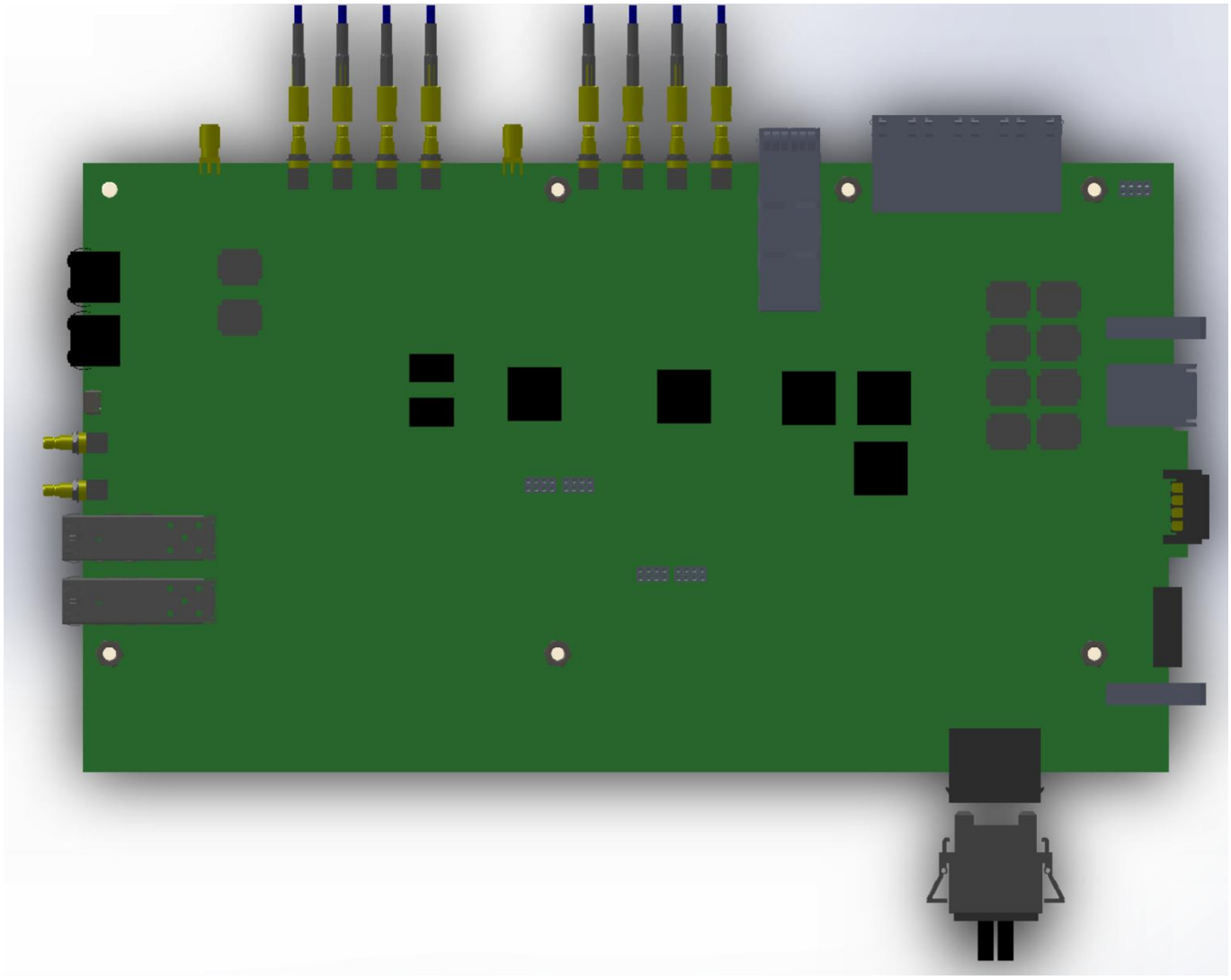


Figure 2. TOP placement and Layout guidelines

The overall generous board size (233x378 mm) allows optimal placement and component separation, for dissipation and isolation issues.
For the clock layout, the bottom side will be preferred for all the RF critical devices.

All the digital circuits, excluding some low power memories, will be placed on the top side to simplify the board assembly and testing.

4.3 Part list, integrated circuits

Reference	Part number	Description
U1	MCIMX6Q5EYM10AD	iMX6 ARM9 Dual Core CPU
U2	LCMXO3LF-9400E-6BG256C	MachXO3-CPLD
U3	ATSAM4S8CA-CU	System Monitor MCU
U4,U5	88E6390xxx-BUK2x000	11 Port Ethernet Switch
U6	88X2222-xx-BKP2C000	QSFP interface
U8	N2M400FDB311A3CE	CPU 4Gbyte Flash disk
U9,U10,U11,U12	MT41K128M16JT	CPU DDR3L memories
U21,U22	ADT7408CCPZ-REEL7	I2C Temperature sensors
U23	M25P32-VMW6G	SPI 256 FLASH Mbit memories
U25,U26	24AA025E48	I2C EEprom with Ethernet MAC
U32,U34	24FC512-I/ST	I2C EEprom
U36	M25PX16-VMN6TP	SPI 256 FLASH Mbit memories
U38,U41	ADCLK944BCPZ	RF x4 differential Clock buffer
U39	CDCV304PW	X4 digital Clock buffer
U42	AD9545BCPZ	Digital PLL

Table 1. Part list

ELECTRICAL CHARACTERISTICS

The following tables show the absolute maximum rating and the recommended operating condition of Management board.

Absolute maximum ratings					
	Component	**Min**	**Max**	**Units**	**Note**
Input supply		0	15	Volt	
PPS in		0	4	Volts	CMOS 3.3V
10 MHz clock in		-10	18	dBm	
Front end digital I/O		0	4	Volts	CMOS 3.3V

Table 2. Absolute maximum ratings

Recommended operating conditions					
	Component	**Min**	**Max**	**Units**	**Note**
Input supply		12	24	Volt	DC stabilized
PPS in		3.0	3.6	V	CMOS 3.3V
10 MHz clock in		-6	12	dBm	-
Front end digital I/O		3.0	3.6	V	CMOS 3.3V

Table 3. Recommended operating conditions

5. MANAGEMENT BLOCK DIAGRAM AND MAIN FUNCTIONS

In this chapter the main Management functions are described. First of all, the board block diagram is shown and commented to help identifying which board physical component(s) cope with each function.
The Management board is proposed in two different configuration: cabinet and Subrack. These two configurations differ mainly for the clock distribution paths, network connections and interface connectors.

5.1 Board Block diagram

The complete block diagram is reported below,

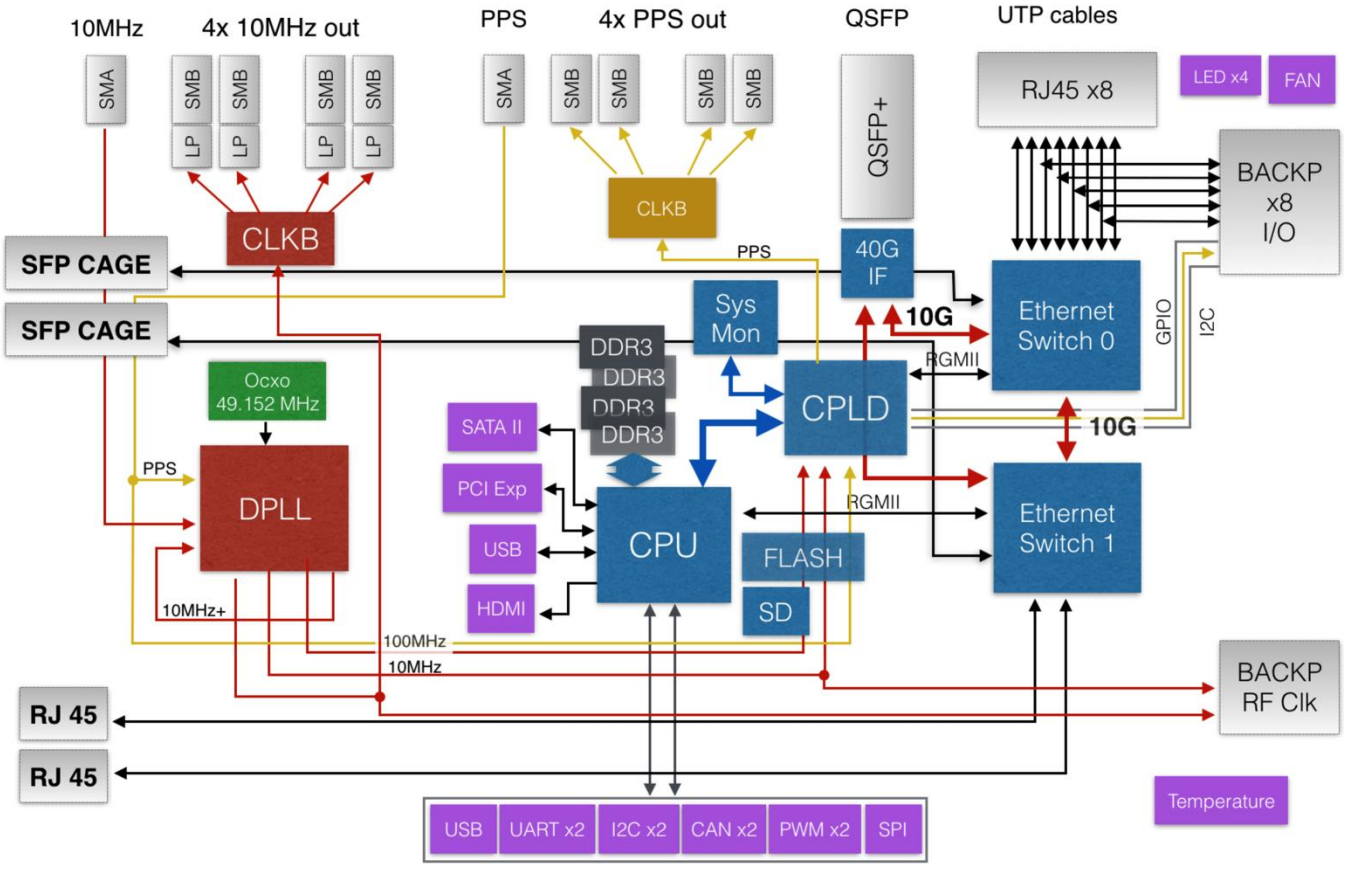


Figure 3. Management Block Diagram

The Management processor board is organized in three areas, from left to right: clock & PPS distribution, CPU and monitoring function and Ethernet function.

The organization of physical components layout into three separate areas has been adopted to obtain performance and noise isolation between DC-DC converter, digital elements and analog interface.

The **clock & PPS distribution** includes the differential x4 RF clock buffer, the Digital PLL (U42) the digital clock buffer(U39) and a selection of 49.152 MHz high quality reference clock.
This clock circuit has been updated on the basis of the clock distribution for LFAA cabinet feasibility study preliminary results selecting the previous active mode for the 10 MHz distribution and an hybrid passive mode for the PPS distribution.

The previously proposed PPS ENCODE function has been dismissed because of the DPLL functional limitation that doesn't allow to manage the phase relationship of the ENCODED signal and the PPS input signal.

The final design will implement the ACTIVE 10 MHZ clock distribution circuit, with the optimal Jitter removal and phase control configuration and the passive PPS distribution adding the capability to measure and manage the phase in relation of the incoming 10 MHz reference.

In the **active mode** the Digital PLL is activated to regenerate the 10 MHz reference clock removing the high frequency noise components from the input reference signal. A low pass digital filter can be enabled on the input and only the phase reference information is maintained to the generated output.
This capability will allow better performances on the clock distribution and no dependencies from the incoming clock reference signal high frequency noise or high frequency signal components.
Thanks to that, the high frequency component of the 10MHz signal distributed from the management to the Sub_Racks inside the cabinet will be removed with a Low Pass Filter on the signal source side reducing greatly the possible electromagnetic emission from the required cables.

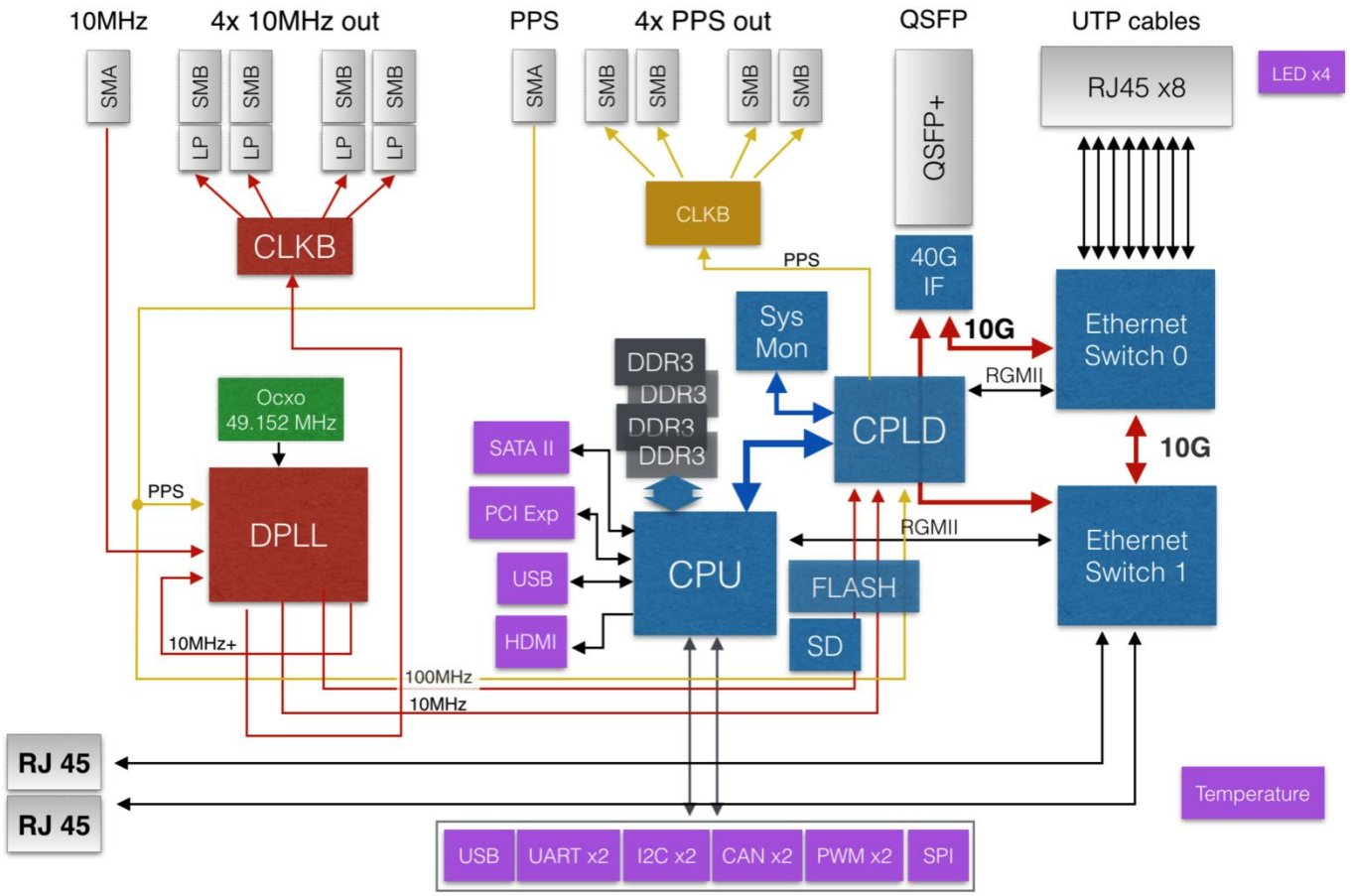


Figure 4 Cabinet management clock configuration

In the cabinet configuration the incoming 10 MHz reference is connected with the DPLL, input A to generate a phase aligned 10 MHz, 100 MHz outputs. One 10 MHz low jitter is routed to the 4x CLOCK BUFFER output that generate 4 synchronous signals, one for each Subrack. Before the clock output connector a Low Pass Filter remove the high frequency component of the signal.
The PPS signal is routed to the DPLL, input B_p and directly to the CPLD. The DPLL generate a 10MHz+ that embed the PPS to the 10MHz reference signal present on the inputA. This generated signal is routed back to the DPLL input B_n to execute a precise phase offset measurement between the PPS edge and the 10 MHz reference closest edge.
The CPLD receive the PPS and shall perform a programmable delay line to move the PPS output phase that is distributed to the Subracks with the dedicate clock buffer.

This circuit shall be implemented in order to measure the PPS phase position at the beginning of the acquisition and adjust the regenerated phase to avoid possible PPS Jumps around a 10 MHz rising edge in the calibration and signal acquisition phase.

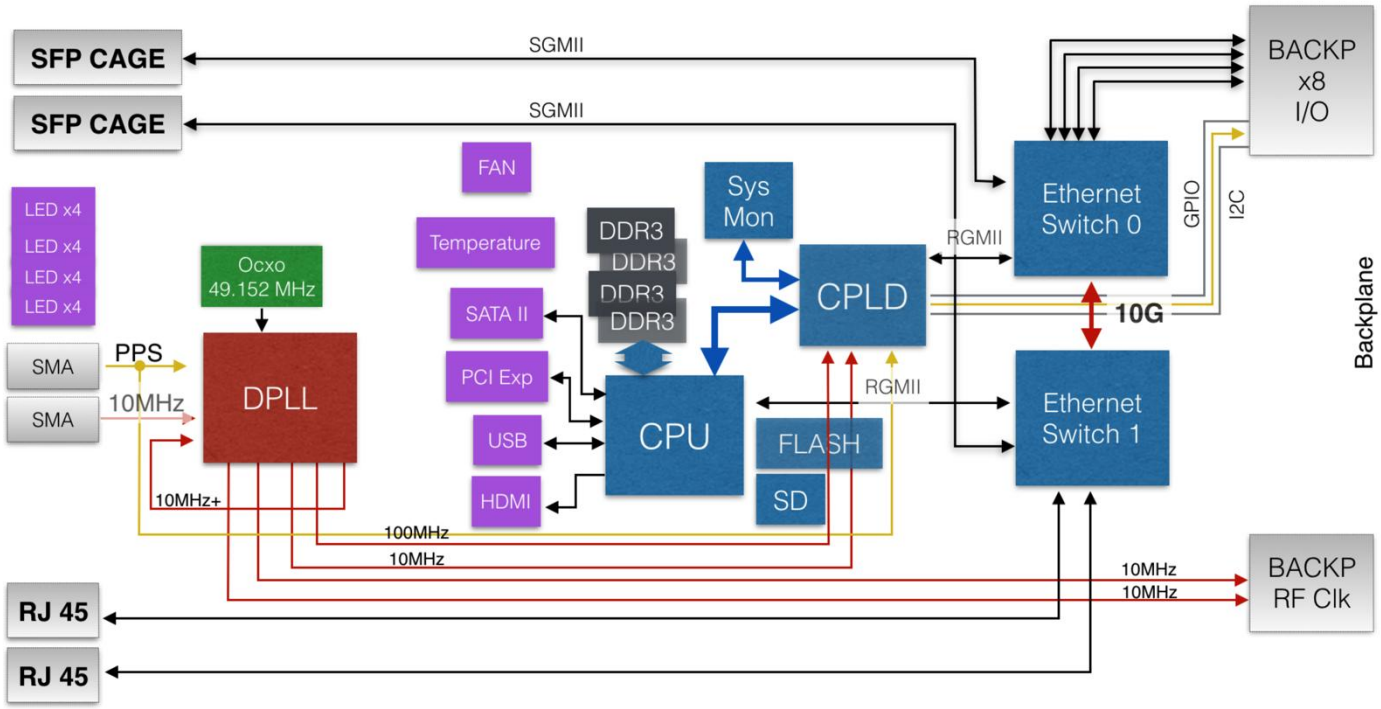


Figure 5 Subrack management clock configuration

In the Subrack management board the clock configuration is similar but the generated 10 MHz by the DPLL are two and routed directly to the backplane.
The PPS generated by the CPLD is routed to the backplane with two signals to the high density backplane I/O connector.

In the Subrack and cabinet integration operation a time of flight of the 10 MHz reference signal and the PPS signal shall be measured and characterized and the cabinet management software shall manage the PPS CPLD delay circuit in order to ensure a stable acquisition.

The **Ethernet** functions are distributed on three main devices: two identical multiport switches (U4, U5) and an optical 40G QSFP interface (U6). Each switch is connected to the other and to the optical QSFP interface with a 10G Xaui interface to create a 18 port gigabit switch with two 10G uplink channel. This architecture guarantees a 10G packet transmission capability from the board to the external network and this configuration is suited to support the Cabinet functionality. Connection diagram is in Figure 6.

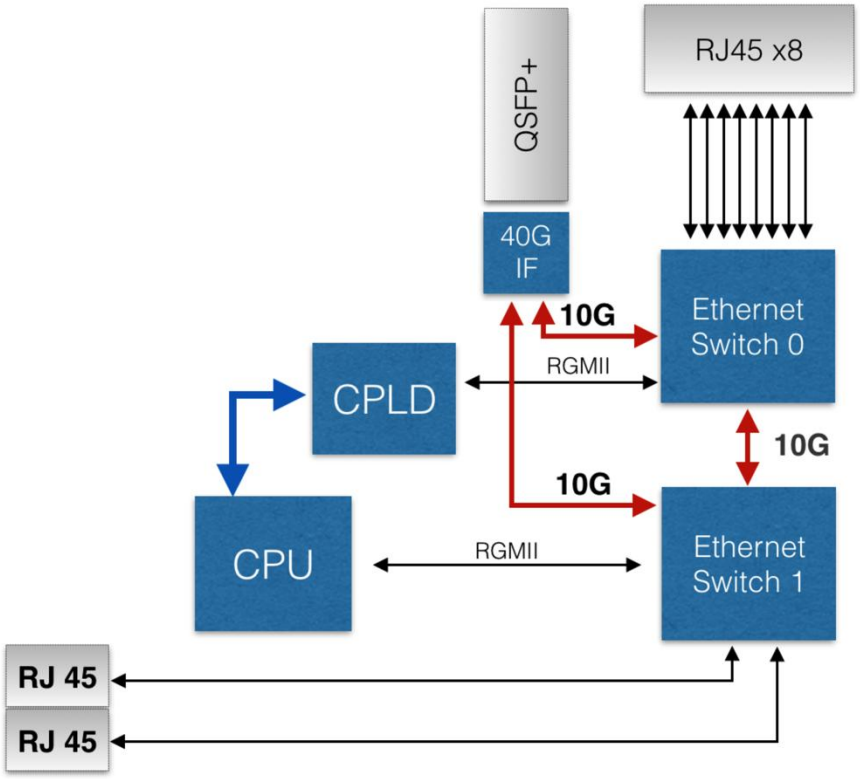


Figure 6 SKA Management Ethernet network, cabinet configuration

The cabinet management network provides also 8 copper interface on the front panel and two copper interface to the rear panel to implement the required cabinet management network (RIF DDD).

In the Subrack configuration the 40G optical interface is not required and the related 10G connections to the switch are reconfigured to implement a single SGMII gigabit link to the SFP cage to add two Gigabit optical fiber interface requested for the Filed Node electronics related to the antennas connected to the Subrack itself.

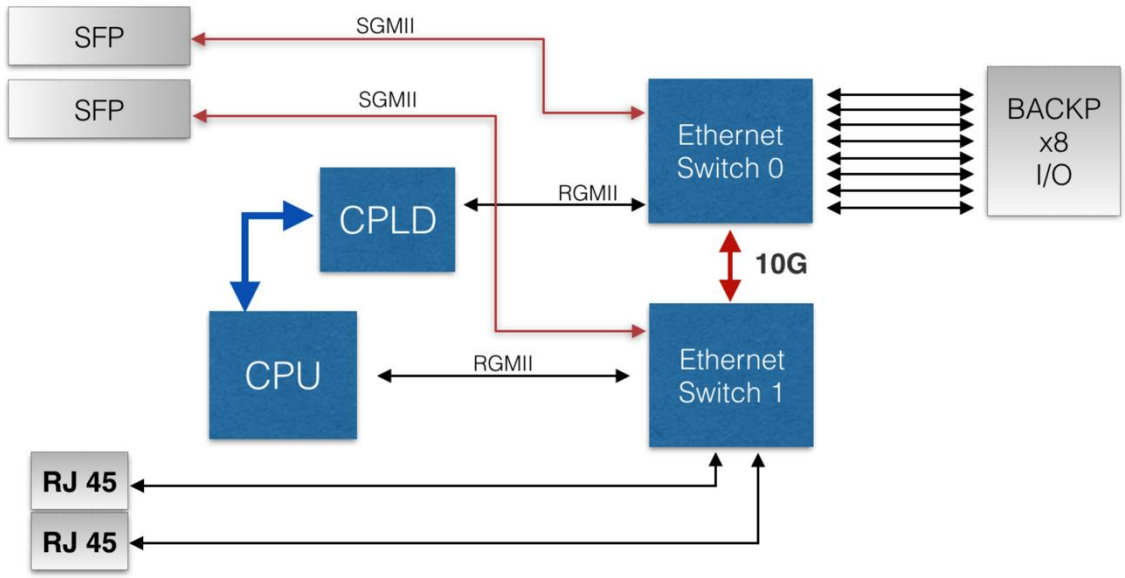


Figure 7 SKA Management Ethernet network, Subrack configuration

In the Subrack configuration the 8 copper interface of the Switch 0 are connected on the backplane high density I/O connector to reach the TPM gigabit interface related to the management network.
The two copper interface of the Switch 1 are available on the front panel to be connected to the cabinet management gigabit network.

The **CPU and monitoring** functions are distributed on three main devices: CPLD (U2), microcontroller (U3) and the main processor (U1).
The CPLD is connected directly to the management network and can implement a low level communication with all the critical system function to ensure system safety.
The microcontroller provide the Analog to Digital interface to measure internal voltages and control some accessories, like fans. The microcontroller is connected with a 8bit data, 14 bit address, memory bus to the CPLD.
The main processor is connected directly to the management network too and also to the CPLD with a memory bus interface. FLASH memories are available (U24, U36) for system boot and data storage. The processor is a dual core Arm9 architecture with several features (Floating point units, Graphical processing Unit, large cache and internal ram memory) and is completed by an external DDR3L memory bank (64 bit wide, 1GByte total capacity) running at frequency up to 533 MHz. For debugging and generic user interface two USB ports and an HDMI video output complete interface are available too.
The SATA II interface available in the CPU is available on a disk-cable connector.
The CPU PCIe interface is available also on a high-speed expansion connector for board capability expansion.
With this architecture the board can provide two IP address, for low level access to the CPLD or high level command interface to the CPU.

6. BOARD POWER SUPPLY

Board power supply is a stabilized DC 12V input. A power monitor and protection circuit is present on the input path to verify the input voltage and limit for over currents.

On the new board revision 1.1 an optional path to plug a battery board has been added in order to implement an auxiliary power supply source to become tolerant to short power missing, as specified in the SKA DDD specification (REF).
The scope of this auxiliary supply shall be:

- maintain the full functions and configuration data for short power missing, TBD the requested time
- in case of long power missing a safe shut-down procedure shall be implemented, saving last configuration data, in order to minimize the following start-up procedure to come back in the acquiring status

7. BOARD EXTERNAL INTERFACES

SKA Management board External interfaces are different for the two configurations, to satisfy the different mechanical specification.
In the Rack configuration the connector on the longer side of the board are populated and the other are unpopulated. Vice-versa in the Subrack configuration.

7.1 Rack Configuration user connectors

A possible final configuration in the Cabinet drawer front end panel is in Figure 8.
From the left to the right the following connector are defined:

- 10 MHz Clock In, SMA, (J28)
- PPS In, SMA, (J32)
- 10 MHz clock Out, SMB, (J26, J27, J29, J30)
- PPS Out, SMB, (J31, J33, J34, J35)
- QSFP+ (U7)
- 8x RJ45 (J7)

User LED x4 are present but not shown in the figure (this will be fixed in the final layout design).

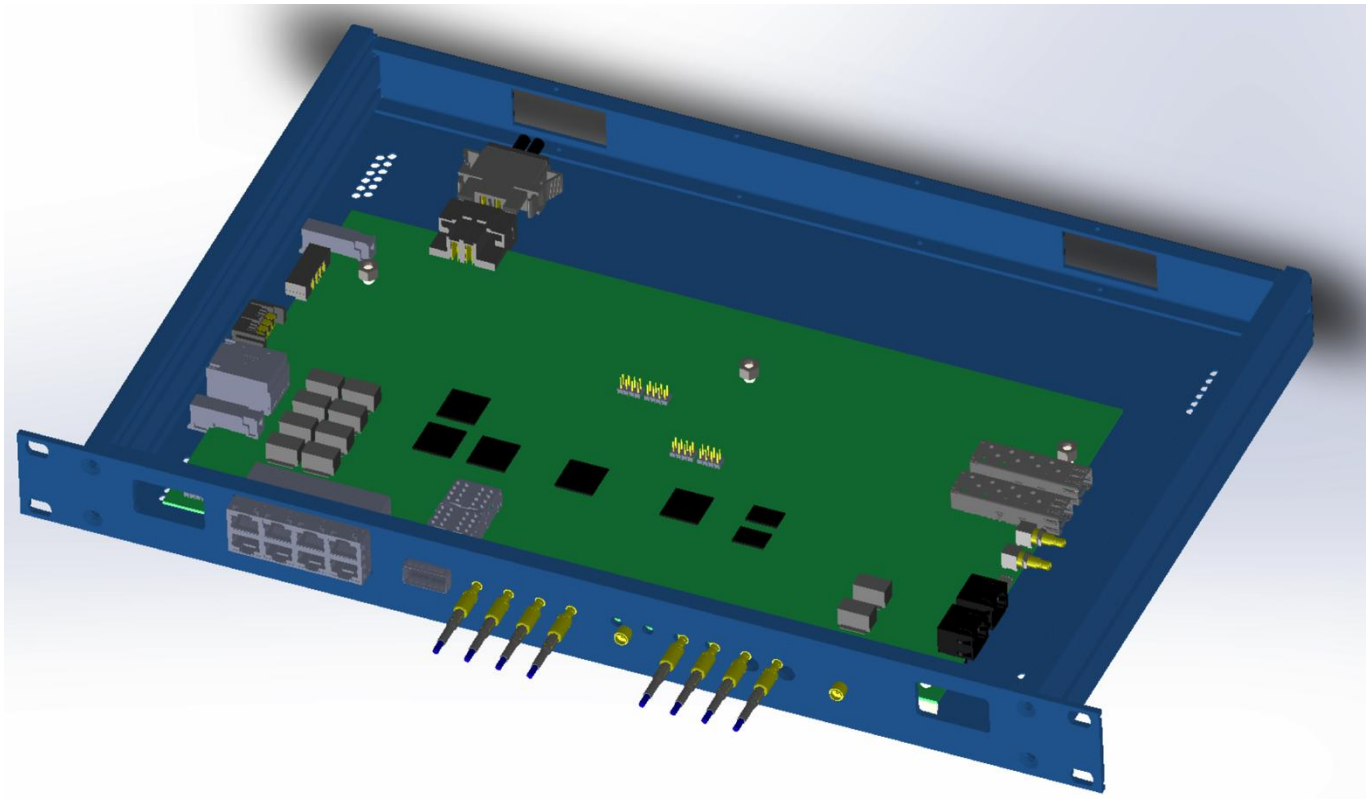


Figure 8 Rack possible installation

The connector on the other side (short side) of the board will be:

- Power In (J2)
- 2x RJ45

- 1x Battery supply module

7.1.1 INTERNAL Connectors and Jumpers

On the TOP side of the Management board other connector are present to add interface to connect other peripheral, debug interfaces and a direct FAN connector.

Reference	Part number	Description
J10	QSH-030	CPU JTAG & TRACE PORT
J11	HEADER 3X2	CPLD JTAG
J12	HEADER 8X2	40G OPTICAL TEST PORT
J13	HEADER 10X2	SYSTEM MONITOR JTAG
J14	HEADER 3X2	SYSTEM MONITOR TEST
J15	HEADER 16X2	I/O EXPANSION
J18	SATA	Hard disk cable interface
J19	QSE014	B2B PCIe and I/O expansion
J20	MMC/SD	SD CARD HOLDER
J21	HEADER 3X2	USER JUMPERS
J22	HDMI	CPU VIDEO OUT
J23	USB	CPU USB OTG 2.0
J24	USB	CPU USB 2.0
J25, J26	HEADER 1X4	ETHERNET USER TEST PORT
J27	47053-1000	FAN supply & control

Table 4. INTERNAL Connectors and jumpers

The J15, I/O expansion, provide the connection to several bus interface on a easy to use, 2,54 mm pin header connector. With this interface is possible to extend the front end feature with an expansion board to be placed to the rear of the drawer to connect several type of instruments.

The detailed connection proposed is in Figure 9.

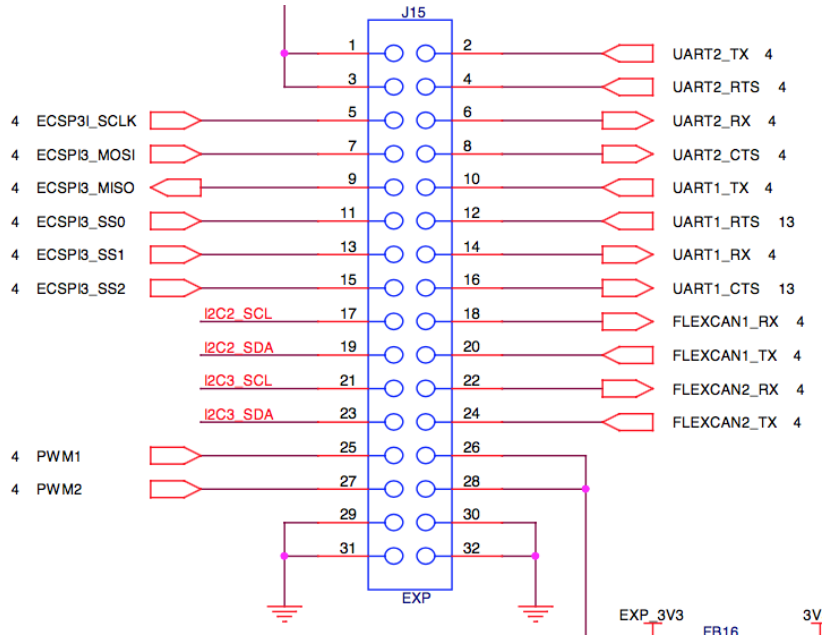


Figure 9 J15 I/O expansion connector

The following peripheral are proposed:

Pins	peripheral	Connection source
1,3	Supply	General supply (Vin or 5v0)
2,4,6,8	UART 2	CPU
5,7,9,11,13,15	SPI high speed	CPU
10,12,14,16	UART 1	CPU
17,19	I2C2	CPU
18,20	CAN1	CPU
21,23	I2C3	CPU
22,24	CAN2	CPU
25,27	PWM1/2	CPU
26,28		General 3v3
29,30,31,32	Ground	General Ground

The physical layer of the listed interface is not present on the Management board and shall be provided, if required, in the optional expansion board.

7.2 Subrack Configuration user connector

The proposed solution for Subrack configuration provides user accessible panel connectors and backplane connectors.

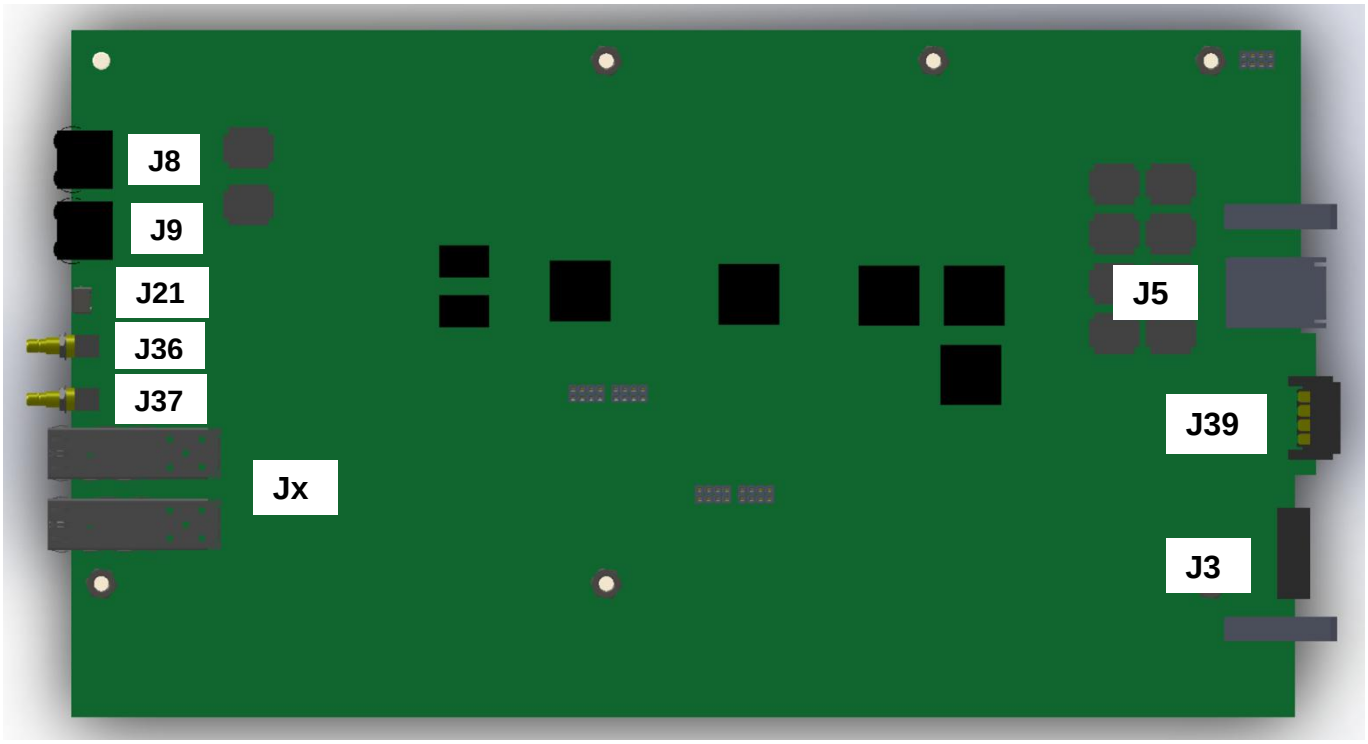


Figure 10 Subrack configuration User Connectors

Reference	Part number	Description
J3	UPT-04-01-01-L-RA-LC-TR	Backplane supply, 10A, 4x
J5	EBTF-4-10-2.0-S-RA-1	Backplane I/O, 8x
Jx1, Jx2	TBD, SFP Cage	Optical Ethernet Gigabit interfaces
J8, J9	RJHSE-5381	Ethernet RJ45
J36, J37	SMB	10 MHz & PPS inputs
J39	IP5_04_RA	Backplane 10 MHz references

8. POWER BUDGET

SKA Management power budget assume a input 12 DC power supply.
The power estimated for the CPU is function of the user software running on it. From the CPU user guide, the power required from different application can vary from 2,5W to the 7W of the more intense one, with all function activated (like the GPU for 3D graphics). In the Management function it is expected that the total power will be less of 5W for typical management application.

	Configuration	
Peripheral	**Rack**	**Subrack x8**
Digital IC		
CPLD	2,5	2,5
CPU & DDR	5	5
40G Optical Ethernet	7	0
Ethernet Switch	3,3	6,6
Other	1,5	1,5
Synchronization		
CLKBuff, PPS buff	0,6	0
DPLL	0,6	0,6
Power distribution efficiency:		
Digital:	86%	
Analog (150 mV linear drop):	79%	
TOTAL DIGIT IC, Watt:	22,3	18,0
TOTAL ANALOG IC, Watt:	1,5	0,7
TOTAL Supply, Watt:	**23,8**	**18,7**

9. BOARD REVISION DIFFERENCES

The differences between board revision 1.0 and the revision 1.1 are listed below:

- new mechanical size, increased board length
- updated Clock and PPS distribution circuit, no component changes
- added Low Pass Filter on the clock output buffers lines
- added 2 gigabit ethernet SFP interface in the Subrack configuration
- removed the 12x TPM backplane interface capability
- added the capability to integrate a battery power unit

END OF DOCUMENT